

Applicant: FLETCHER, Thomas D
Serial No. 10/020,447
Response to Office Action mailed June 7, 2005

REMARKS

1. Introduction

Claims 10-25 and 32-42 are pending in this application. (Claims 1-9 and 26-31 have been withdrawn.) Claims 32 and 37 have been amended. Claim 40 has been cancelled. Claims 10, 13, 17 and 19 were rejected as anticipated by Ware (U.S. Pat. No. 4,623,982), and claims 14, 22-25, 32, 34-35, 37, and 40-41 were rejected as obvious over Ware. Claims 11 and 18 were rejected as obvious over Ware in view of Vo (U.S. Pat. No. 4,737,926).

2. Claims 10-25 are believed to be patentable over Ware and Vo

With respect to claim 10, it is noted that a carry generation block is to determine exactly three of the carry-out values. A carry-out value is defined earlier in the claim as being determined for each propagate value based on the propagate value and the corresponding generate value. Accordingly, three carry-out values being generated by a carry generation block would require three propagate values. The current Office Action provides a marked up version of Fig. 3A from Ware. Of course, Ware describes the entire circuit of Figure 3A as a "block" with three individual cells (i.e., a start cell, a continue cell, and an end cell). In the drawing, the selective parts of the circuit are circled and denoted as a "carry generation block." Applicant respectfully disagrees. If C IN 0 (1), C IN 1 (1), and C IN (1) are to be denoted as carry-out values, then according to the claim, each carry-out value would be determined for each propagate value based on the propagate value and the corresponding generate value. Looking at the circled circuit of Fig. 3A, propagate signal P(1) is an "input" to this denoted circuit. No other propagate signals would be inputs to this denoted circuit. Accordingly, the circuit labeled "carry generation block" does not generate three carry-out values, each being determined for each propagate value as recited in claim 10. Likewise, claim 17 recites a carry generation block that is connected to exactly three of the propagate outputs and three of the generate outputs, and the carry generation block has a plurality of carry

Applicant: FLETCHER, Thomas D
Serial No. 10/020,447
Response to Office Action mailed June 7, 2005

outputs. As indicated above, the circuit labeled "carry generation block" has only one propagate input, not three.

As to the rejection of claims 11 and 18 under 35 U.S.C. § 103(a), Vo fails to make up for the deficiencies of Vo. In Vo, each individual bit adder 61 in Fig. 5 is to take in two bits to add and a carry in from the previous bit adder and generate a carry out for the next bit adder. There is no disclosure in Vo or Ware of a carry generation block that determines exactly six of the carry out values as described in claims 11 and 18.

As to the rejection of claim 32, this claim has been amended to bring out the definition of taper. such a feature is not shown or suggested by the cited references. Accordingly reconsideration and withdrawal of the rejection of claim 32 and 34-35 under 35 U.S.C. § 103(a) is respectfully requested.

As to the rejection of claim 37, this claim has been amended to include the limitation of claim 40. The Office Action states that there is "one critical path through the carry generation blocks" shown in Fig. 3B of Ware. It is noted that there is no mention of a "critical path" in Ware. Even assuming, arguendo, that the path between C IN ADDER to C OUT BLOCK (3) is a critical path, there is no disclosure or suggestion in Ware to include buffer inputs and outputs of gates on such a path to reduce the load on the path as recited in the claim. In view of the above, reconsideration and withdrawal of the rejection of claims 37-39 and 41-42 is respectfully requested.

In view of the above, reconsideration and withdrawal of the rejection of claims 10-25 and 32-42 is respectfully requested.

Applicant: FLETCHER, Thomas D
Serial No. 10/020,447
Response to Office Action mailed June 7, 2005


3. Conclusion

Applicant respectfully requests entry of the above amendments and favorable action in connection with this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. 1.16 or 1.17 to Kenyon & Kenyon Deposit Account No. 11-0600. The Examiner is invited to contact the undersigned at (202) 220-4255 to discuss any matter concerning this application.

Respectfully submitted,

Kenyon & Kenyon

Date: June 7, 2005


Shawn W. O'Dowd
Registration No. 34,687
(Attorney for Intel Corporation)

KENYON & KENYON
1500 K Street, N.W.
Washington, D.C. 20005
Ph.: (202) 220-4200
Fax.: (202) 220-4201
DC1-592624